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# A New Approach to Design of Cost-Efficient Reversible Quantum Dual-Full Adder and Subtractor

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**Abstract**
This paper proposed the design and development of reversible cost-efficient innovative quantum dual-full adder and subtractor or QD-FAS circuit using quantum gate. The proposed circuit can be used as full adder and full subtractor simultaneously, which is

designed using double Peres gate or DPG and Feynman gate or FG. The quantum cost, garbage output and constant input of the QD-FAS is 8, 1 and 1. Which is better w.r.t previously reported work. The QD-FAS circuit, as proposed, includes shared sum and difference terminals, as well as a carry-out and a borrow output terminal. Notably, this innovation showcases a remarkable 27.27% reduction in quantum cost. The improvement in garbage output is even more striking, showing a 50% enhancement. When assessing the overall advancement in quantum cost, it falls within the range of 27.27% to 66.66%. To confirm the viability of this design, extensive testing is carried out using the IBM Qiskit simulator. This design holds significant importance in a variety of applications, including quantum computing, cryptography, and the realm of reversible Arithmetic Logic Units (ALU).

**Keywords-** Reversible logic gate, Quantum cost, Adder, Subtractor, Qiskit.

## 1. Introduction

In the realm of reversible logic design and implementation, several key parameters hold significant importance, including quantum cost (QC), garbage output (GO), constant input (CI), and delay (D) (Kianpour & Sabbaghi-Nadooshan, 2017; Maity et al., 2018a; Maity et al., 2018b; Kumar & Singh, 2019). The quantum cost of a circuit is determined by the overall count of elementary quantum gates required to implement the specified function. The core principle underpinning reversible circuits lies in their design, allowing digital circuits to perform computations while retaining all information (Zhou et al., 2000; Zhang et al., 2004; Znidaric et al., 2008).

Within the realm of reversible circuits:

a. Information Preservation: Each input corresponds to a unique output, and vice versa. As a result, no data is lost during computation, and in theory, the original inputs can be fully recovered from the outputs.
b. No Energy Loss: Reversible circuits are engineered to minimize energy dissipation, including the generation of heat or other forms of energy loss. This differs from classical irreversible circuits, where energy is dissipated as heat, especially when bits are erased (e.g., in AND or OR gates).
c. Input-Output Balance: In a reversible circuit, the number of input bits precisely matches the number of output bits.
d. Deterministic Operations: Reversible gates execute operations in a deterministic manner, devoid of the probabilistic actions commonly found in quantum computing.
e. Quantum Computing Relevance: Reversible circuits are of significant importance in quantum computing. Quantum gates, inherently reversible, preserve quantum information, and quantum computers use reversible operations to manipulate quantum states.
f. Low Power Utilization: Reversible circuits are attractive for specific low-power applications as they minimize energy dissipation.

This research paper introduces the design of a dual-full adder and subtractor, known as the QD-FAS circuit with optimized for QC, GO, and CI, and created using reversible logic gates. The validity of this proposed circuit is confirmed through experimentation using the IBM Qiskit simulator.

The categorization of the remaining paper is outlined as follows: Section 2 presents the literature review. Section 3 encompasses a basic concept focused on reversible logic functions, reversible logic gates and its applications. Section 4, presents the proposed circuits, while section 5 addresses its simulation results. Section 6 presents the concluding remarks of the proposed works.

## 2. Literature Review

Reversible circuits find applications in various domains, including quantum computing, cryptography, the design of energy-efficient circuits, and specialized computational tasks where information preservation and energy conservation are paramount. They serve as a foundational concept for understanding the theoretical

limits of computation and information processing (Chau & Wilczek, 1995; Naghibzadeh & Houshmand, 2017; Bhat et al., 2023).

The central objective when working with reversible logic is to minimize these parameters. While many researchers have introduced diverse reversible combinational logic circuits, there has been relatively limited progress in the development of reversible adder-subtractor designs. Nevertheless, it is feasible to construct all the aforementioned circuits using fundamental reversible logic gates.

The quantum dual-full adder and subtractor circuits were introduced by Moghimi & Reshadinezhad (2015) with QC 11. Similarly, Thersesal et al. (2015) present the same circuit with QC 14. Gupta et al. (2013) proposed the quantum dual-full adder and subtactor with QC 19. Rangaraju et al. (2011) and Moghimi & Reshadinezhad (2015) independently proposed the same circuit in with QC 21 and 24 respectively. Bazmalah & Kamal (2022) proposed the same circuit with QC 12.

## 3. Basic Concepts

Reversible logic functions are characterized by having an equal count of inputs and outputs (Banik & Rahaman, 2023; Smolin & DiVincenzo, 1996; Vedral et al., 1996). Reversible gates, in particular, exhibit this symmetry with an AxA representation, where 'A' signifies the number of inputs and outputs. For an input vector denoted as (IA1, IA2,……..IAR), its corresponding output vector is represented as (OA1, OA2,……OAR). As illustrated in Figure 1, you can observe a concrete example of an A×A reversible logic gate. The key feature of reversible logic gates is the establishment of a one-to-one mapping between inputs and outputs, enabling the retrieval of outputs from inputs and vice versa (Bennett, 1973).

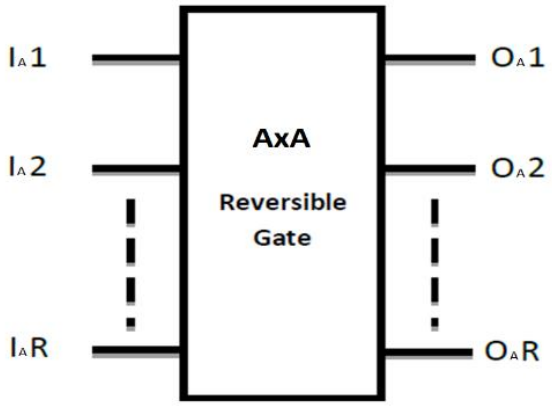


**Figure 1.** Basic A×A reversible logic gate.


**Figure 2.** 1x1 reversible NOT gate.

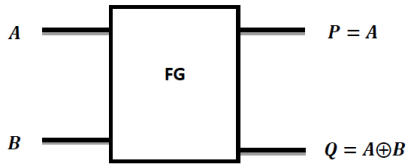


**Figure 3.** 2×2 reversible Feynman gate.

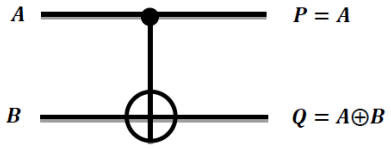


**Figure 4.** Quantum implement of Feynman gate.

Several reversible gates exist, including the reversible NOT gate (Misra et al., 2017), Feynman gate (FG) (Feynman, 1985), Peres gate (PG) (Peres, 1985), double Peres gate (DPG) (Tara & Babu, 2016), Fredkin gate, Toffoli gate (Fredkin & Toffoli, 1982), controlled V gate and controlled V+ gate (Maity, 2022), and more. In the "controlled-V gate, when input A is '0', the output Q is equal to B. Conversely, if A equals '1', the output Q becomes V(B), where, V is defined as the unitary operation $V = \frac{i+1}{2}\begin{pmatrix} 1 & -i \\ -i & 1 \end{pmatrix}$ is applied to the input B. V+ is the Hermitian of V". However, this paper focuses exclusively on the reversible Feynman gate and double Peres gate. In Figure 2, you can observe the 1×1 reversible NOT gate with a quantum cost of 0. Here, A serves as the input terminal, and P represents the output terminal, with P being the complement of A (P=A').

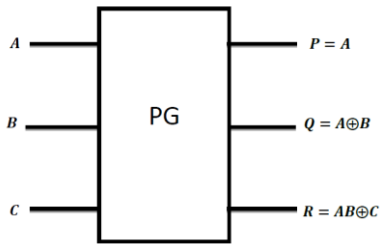


**Figure 5.** 3×3 Peres gate.

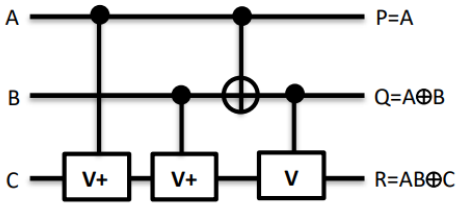


**Figure 6.** Quantum implementation of Peres gate.

Figure 3 displays the fundamental block diagram of a 2x2 Feynman gate, as depicted in Figure. 4. This gate is represented in its quantum form with a quantum cost (QC) of 1. It takes input signals from terminals A and B and yields outputs at P and Q (P=A, Q=A ⊕ B). Moving on to Figure 5 and Figure 6, we encounter the 3x3 Peres gate, characterized by a QC of 4. This gate receives input signals from terminals A, B, and C, producing outputs at P=A, Q=A ⊕ B, and R=AB ⊕ C. Figure 7 and Figure 8 introduce the 4x4 Double Peres gate (DPG), which has a QC of 6. It involves input terminals A, B, C, and D, and generates outputs at P=A, Q=A ⊕ B, R=A ⊕ B ⊕ D, and S=(A ⊕ B)D ⊕ AB ⊕ C.

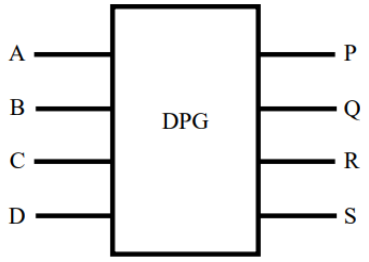


**Figure 7.** 4×4 Double Peres gate.

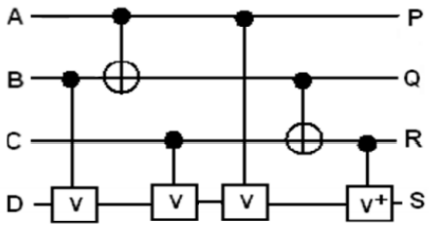


**Figure 8.** Quantum implementation of double Peres gate.

## 4. Proposed Quantum Dual-Full Adder and Subtractor or QD-FAS Circuit

Figure 9 shows the reversible full-adder circuit using a double Peres gate with QC 6, CI 1 and two garbage outputs. If the C input terminal of the DPG is zero, then R output terminal is used as Sum and S output terminal is used as carry output. The P and Q output terminals are two garbage outputs. Table 1 shows the truth table of the full adder. Table 2 shows the QD-FAS truth table, where A, B, $C_{IN}$/$B_{IN}$ are inputs and S/D, $C_{OUT}$, $B_{OUT}$ are the output terminals of the proposed circuit. The $B_{OUT}$ is the XOR operation of A, S/D and $C_{OUT}$, which is find out from Table 3.

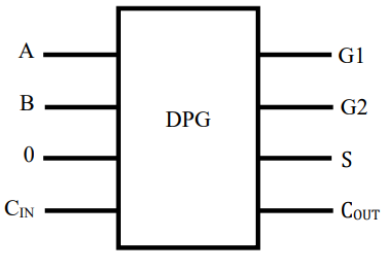


**Figure 9.** Full adder using DPG.

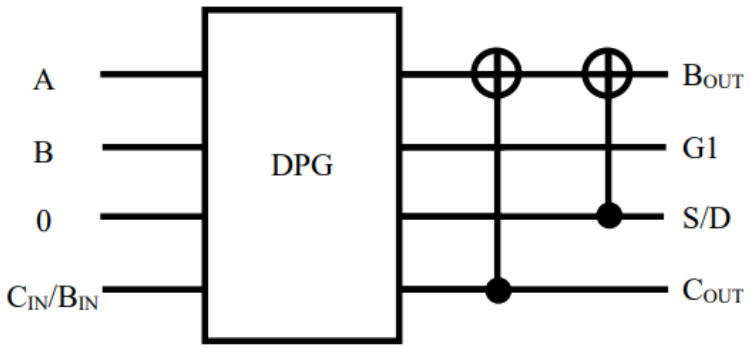


**Figure 10.** Proposed dual-full adder and subtractor using DPG and FG.

Figure 10 displays the suggested QD-FAS circuit with a double Peres gate configuration. This circuit is configured with QC set to '8', CI set to '1', and GO set to '1'. The design of this proposed circuit involves employing one Double Peres Gate (DPG) and two FG, as illustrated in Figure 10.

The input terminals of the Double Peres Gate are utilized as the input for the QD-FAS. The 'C' input is designated as 'CI' with a value of '0', while the 'D' input serves as '$C_{IN}/B_{IN}$'. The output is obtained from the output P, R, and S terminals by passing through two FG, and the result is taken from the 'Q' terminal marked as 'GO'.

For example, the output probability function for the input '0000'is '0000'. The third input is CI and 2nd output is GO, i.e. A=0, B=0, C=CI=0, D= $C_{IN}/B_{IN}$=0, and P=$B_{OUT}$=0, Q=GO=0, R='S/D'=0, S=$C_{OUT}$=0. Similarly, the output probability function for the input '1011'is '1111'. The third input is CI and 2nd output is GO, i.e. A=1, B=1, C=CI=0, D= $C_{IN}/B_{IN}$=1, and P=$B_{OUT}$=1, Q=GO=1, R='S/D'=1, S=$C_{OUT}$=1 [S/D is the output Sum/Difference].

**Table 1.** Truth table of full adder.

| A | B | $C_{IN}$ | S | $C_{OUT}$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

**Table 2.** Truth table of QD-FAS.

| A | B | $C_{IN}/B_{IN}$ | S/D | $C_{OUT}$ | $B_{OUT}$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 |

Simply find out $B_{OUT}$ from Table 2 and Table 3.
$B_{OUT} = A \oplus (S/D) \oplus C_{OUT,}$
$S/D=A \oplus B \oplus (C_{IN}/B_{IN})$,
$C_{OUT}=(A \oplus B)C \oplus AB$,
$B_{OUT}=A \oplus [A \oplus B \oplus (C_{IN}/B_{IN})] \oplus [(A \oplus B)C \oplus AB]$.
After simplification of the above equation
$B_{OUT} = (A\ B)B_{IN} \oplus A'\ B$.

Therefore, QD-FAS can be designed using DPG and FG with quantum cost 8, garbage out 1 and constant input 1. The improvement % of QC and GO of the proposed circuit is 27.27% and 50% respectively w.r.t. previously reported results. Overall, the QC improved 27.27 - 66.66 % with previously reported results. Table 4 shows the comparison result of the proposed circuit.

**Table 3.** Special truth table for finding out $B_{OUT}$.

| A | S/D | $C_{OUT}$ | $B_{OUT}$ |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 |

**Table 4.** Comparison results of proposed QD-FAS using DPG and FG.

| Reference | QC | GO | CI |
|---|---|---|---|
| Proposed Design | 8 | 1 | 1 |
| Moghimi & Reshadinezhad (2015) | 11 | 2 | 0 |
| Bazmalah & Kamal (2022) | 12 | 2 | 1 |
| Thersesal et al. (2015) | 14 | 1 | 2 |
| Gupta et al. (2013) | 19 | 5 | 3 |
| Rangaraju et al. (2011) Design 1 | 21 | 5 | 3 |
| Rangaraju et al. (2011) Design 2 | 14 | 3 | 1 |
| Rangaraju et al. (2011) Design 3 | 10 | 3 | 1 |
| Morrison & Ranganathan (2011) | 24 | 4 | 5 |
| Overall Improvement % | 27.27 – 66.66 | 0 – 80 | 0 – 80 |

## 5. Simulation Results

This portion presents the simulation results of proposed reversible QD-FAS circuits. Figure 11 illustrates the quantum realization of the suggested circuit, while Figure 12 displays the simulation outcomes showing the output probability through IBM Qiskit. This serves as confirmation for the proposed circuit. In Figure 13, we can see the output probability function for the input A=0, B=0, and $C_{IN}/B_{IN}$=0', with S/D as '0', $C_{OUT}$ as '0', 2nd qubit GO '0', and $B_{OUT}$ as '0'. This output function aligns with the truth table, as confirmed. Likewise, in Figure 14, the output probability function for the output '1111' [2nd qubit GO '1'] as the input, with S/D at '1', $C_{OUT}$ at '1', and $B_{OUT}$ at '1' is shown. All these output results have been validated using the IBM Qiskit simulator.

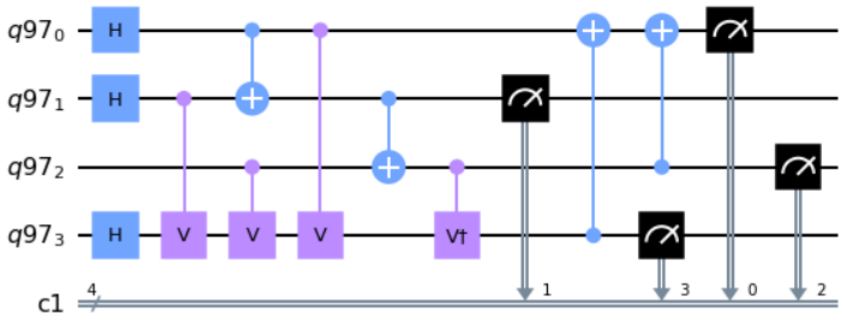


**Figure 11.** Quantum circuit of proposed QD-FAS using IBM Qiskit.

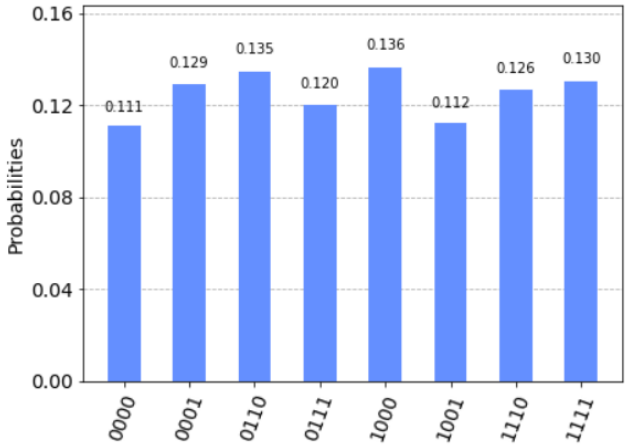


**Figure 12.** Simulation results of the Proposed QD-FAS.

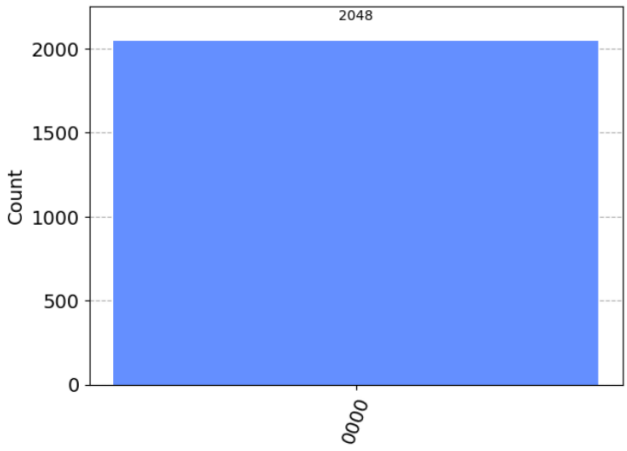


**Figure 13.** Output probability function of the output '000', when input is '000', and 2nd qubit is GO '0'.

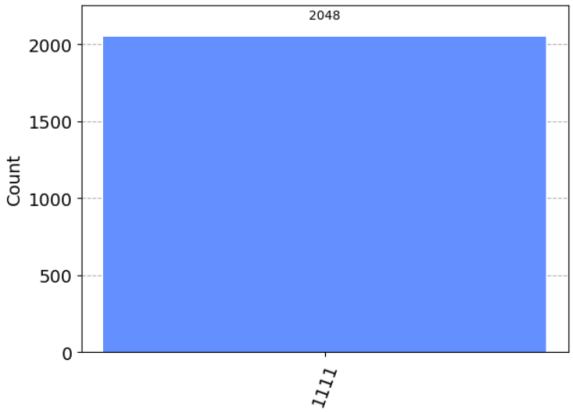


**Figure 14.** Output probability function of the output '111', when input is '111' and 2nd qubit is GO '1'.

## 6. Conclusion

The author introduces a novel approach for designing a quantum double-full adder and subtractor (QD-FAS), with a specific focus on optimizing QC, GO, and CI using quantum gates. This circuit serves the dual purpose of functioning as both a full adder and a full subtractor. The QC, GO, and CI values for the QD-FAS are 8, 1, and 1, respectively. The proposed QD-FAS circuit incorporates common sum/difference terminals, alongside a carry-out and a borrow output terminal. Notably, the proposed work demonstrates a substantial 27.27% improvement in quantum cost. The enhancement in the case of garbage output is an impressive 50%. When considering overall quantum cost improvement, it ranges from 27.27% to 66.66%. So, the proposed work is cost effective compared to previous work. To validate the proposed design, the work is rigorously tested using the IBM Qiskit simulator. This design holds significant relevance in various applications, including quantum algorithms, quantum error correction, quantum data compression, quantum arithmetic, quantum cryptography, quantum random number generation, and reversible Arithmetic Logic Units (ALU).

### Conflict of Interest

There are no conflicts of interest to disclose in connection with this publication.

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