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Packed U Cell Seven Level and Five Level Inverter Topologies for Renewable Energy Applications

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Abstract
The multilevel inverter (MLI) is a power electronic circuit applied for power and voltage applications. It has the advantages of minimum total harmonic distortion (THD), less voltage stress on the switching devices, fewer switching losses, and a smaller size of passive filters. These high-level inverters are applied in applications like AC drives, FACTS, and in the field of renewable energy. There are various inverters for such applications. A PUC multilevel inverter contains fewer components, fewer switching losses, and easy-to-balance voltage on capacitor sides. In this paper, the performance of the transformer less seven-level inverter and the five-level inverter is analyzed. The sinusoidal pulse width modulation (PWM) has been used with this PUC-based structure. The new control strategy is designed to reduce harmonic contents and low filter ratings. A relative analysis is carried out to focus on the superiority of the recently developed packed U-cell topology. The performance of packed U-cell, seven-level, and five-level inverters has been compared. These types of inverters consist of two power switches and a single capacitor to make this inverter effective. The PUC 7 inverter contains a lot of sensors and other control components to balance the voltage on the capacitor side

by one-third of the input voltage, so the structure becomes complex. While PUC 5 is sensor less technology, there is no voltage balancing issue and no complexity found in this inverter. In PUC5, the only level is low, but it is very easy to interface with grids and other devices. So it is the most preferable as compared to PUC7. The performance analyses of these inverters have been verified through simulation.

Keywords- Multilevel inverter, Packed U-cell, Sensor-less controller, Renewable energy.

1. Introduction

Connecting one power semiconductor switch straight to low voltage grids is difficult due to its low rating, due to switching losses, the need for a switch with very little turn-on and turn-off time, the issue of voltage sharing in series connected devices, and the higher order harmonics (Rodriguez et al., 2002). For more than three decades, multilevel inverters have been under investigation and production. This technology is still under development, however, in the last few years, several new contributions and topologies have been published. Due to their advantages over traditional two-level pulse-width-modulated (PWM) inverters, multilevel inverters have recently become more appealing to researchers.

For these purposes, operating with higher voltage levels has emerged as a new family of multilevel inverters. Multilevel inverters have attracted growing interest in business and academia for high-power applications as one of the most favored electronic power conversion solutions (Franquelo et al., 2008). They have successfully entered the market and can thus be regarded as a mature and tested technology. They are currently available in regular items that supply a wide variety of applications. Multilevel inverters are defined as inverters with output voltages of more than two degrees (Rodriguez et al., 2009). So, the inverter's output voltages have a lower THD and higher efficiency. The devices are also limited to a fraction of the DC-link voltage (Lakshmi et al., 2013). These features make it possible to adopt multilevel inverters for high-power applications. Over the last two decades, novel converter topologies and special modulation schemes have been involved in contemporary studies (Gupta et al., 2015). In addition, in the literature, three major multilevel inverter structures were stated as follows: cascaded H-bridge inverters (CHBI), diode clamped, and flying capacitor inverters. One of the successful multilevel topologies is the cascade multilevel inverter (CMLI) (Jalakanuru and Kiber, 2017). In fact, CMLI has a high degree of modularity compared to other multilevel-based topologies, because each inverter may be viewed as a module with comparable architecture, control structure, and circuit modulation (Ahamad and Ansari, 2021).

For small- and normal-power applications, such as connecting solar panels to the local grid for residential use or street lighting, multilevel inverter topologies can also be used to convert the DC voltage of the renewable energy resource into an appropriate AC waveform that can be used at the load and grid sides (Alishah et al., 2017).

It is preferable in these situations to use a single-phase transformer-less inverter with the fewest possible DC sources (Sabhaya and Sheth, 2015). Initially, we presented the packed U-cell (PUC) inverter, which produces seven different voltage levels with just six active switches, one isolated DC source, and one capacitor serving as a second source, whose voltage needs to be adjusted to stabilize at one-third of the first DC source (Niu et al., 2019).

Basically, shunt active filters are used in packed U-cell-type inverters. The control technique is planned to decrease the harmonic content of the load voltage. Like these converters, filters' ratings are considerably low. This affects very much the efficiency of power exchange and the cost of the installations (Sharifzadeh and Al-Haddad, 2019).

The summary table for the literature review is described in **Table 1**.

Table 1. Summary table for literature review.

Author & Year	Objectives	Methodology	Key Findings	Limitations
Ounejjar et al. (2010)	Compare performance of Packed U cell 5-level and 7-level inverters	Simulation using MATLAB/Simulink	7-level inverter shows higher efficiency at low loads, while 5-level excels at high loads	Limited to simulation results, real-world validation needed
Leon et al. (2016)	Investigate the impact of modulation techniques on output quality	Experimental setup with a prototype inverter	Sinusoidal PWM yields lower THD in the 7-level, but the 5-level exhibits a better transient response	Small-scale experiment, scalability concerns
Siddique et al. (2019)	Analyze the economic feasibility and control of implementing Packed U cell inverters	Cost-benefit analysis and financial modeling	The initial investment for 7-level is higher, but long-term operational cost favors 7-level in specific applications	Economic conditions and assumptions may vary
Sharifzadeh and Al-Haddad (2019)	Explore the reliability and fault tolerance of both inverters	Reliability modeling and fault simulation	5-level inverter shows better fault tolerance under certain conditions, while 7-level has advantages in others	Limited fault scenarios considered, real-world testing required
Khoshhava et al. (2023)	Review advancements in control strategies for Packed U-cell inverters	Literature review and comparative analysis	Predictive control enhances the performance of both inverters, but challenges remain in real-time implementation	Focus on control strategies, application-specific nuances not covered

The major minus of inverters, however, is the use of several switch numbers (Ajami et al., 2019). Not only does this raise costs, but it also affects the harmonic content. For this study, this is the main motivation. Switching losses are significant, in part because they are dependent on the modulation method; they can therefore be adjusted for a given topology through the selection of the modulation scheme and parameter design (Khoshhava et al., 2023). The harmonics produced by the converter also harm the efficiency in addition to the switching losses and must therefore also be taken into account (Ahamad et al., 2020).

The novelty of this paper is to introduce a new self-voltage-balancing sensor-less 5-level PUC inverter called sensor-less PUC5 that has been proposed as a result of research into PUC topology to have a simpler controller and better performance (Ounejjar et al., 2010). Using a self-voltage-balancing mechanism built into the multicarrier pulse width modulation (PWM), the PUC5 inverter capacitor voltage would be fixed at half of the DC source amplitude (Kamaldeep and Kumar, 2015). There is no requirement for voltage or current sensors because complex controllers are not used. Less harmonic distortion and a symmetric five-level output voltage waveform would result from maintaining the capacitor voltage at the desired level (Prabaharan and Palanisamy, 2016). While the PUC 7-level inverter contains a lot of sensors to control this inverter to balance voltage.

- Propose a novel multilevel competitive topology that offers high power quality using a small number of passive and active components.
- The novel topology can be seen as a packed U-cell inverter.
- Compared to the seven-level PUC inverter, the five-level PUC inverter is cost-effective and due to self-voltage balancing, easy to control.

If we compare the PUC inverters with other types of inverters like flying capacitors type, diode clamped types, cascaded types, or other hybrid-type inverters, all these types of inverters contain a larger number of components, while PUC-type inverters for the same level contain a smaller number of components with good quality of output voltage, a lower THD, and high-efficiency performance. This type of inverter can be operated in both converter modes, like DC-AC or AC-DC. These types of converters occupied two high-performance switches and one capacitor. While the other two switches are used for low-frequency values to maintain and alternate the positive and negative voltage sequences. Initially, PUC series inverters, the

first PUC7 were introduced, but due to some drawbacks in incorporating them with industries, they are not preferable, while the level is good. All these types of drawbacks are overcome in the PUC5-level inverter that is incorporated in PUC5 due to smooth control operation and easy-to-maintain voltage balancing across the capacitor. The voltage across the capacitor is to maintain half of the source voltage for generating 5 levels. The controller is designed to be ideal and robust for smooth operation if there are any uncertainties on the source side or load sides of the PUC5 implementation. So, we can state that the PUC5 inverter can solve multi-objective control problems. There is a reverse relationship between capacitance and frequency that directly depends on the size of the capacitor. The proposed method is used to balance the voltage that directly influences the size of the capacitor in the PUC 5 inverter.

The work is organized as follows: section 2 discusses the flow chart of the proposed approach step-by-step. In section 3, the control design, operation technique, and result of the PUC7 inverter are described. In section 4, the control switching technique, development of the self-balancing voltage controller, operation procedure, and simulation results are given. In section 5, a cost-saving analysis is given. In section 6, a comparison analysis of both inverters is given on the basis of control complexity and components used. Finally, the conclusions section summarizes and discusses the obtained results.

2. Proposed Approach

An algorithm is described in this paper by providing a detailed explanation of the steps involved in accomplishing a specific task. This paper includes information about the complexity and cost-saving inverter of the algorithm (Taghvaie et al., 2017). Basically, the main aim of this research is to develop a very low-cost inverter with low control complexity and a comparison analysis of cost savings. So, the proposed work is shown by the flow chart as given in **Figure 1**.

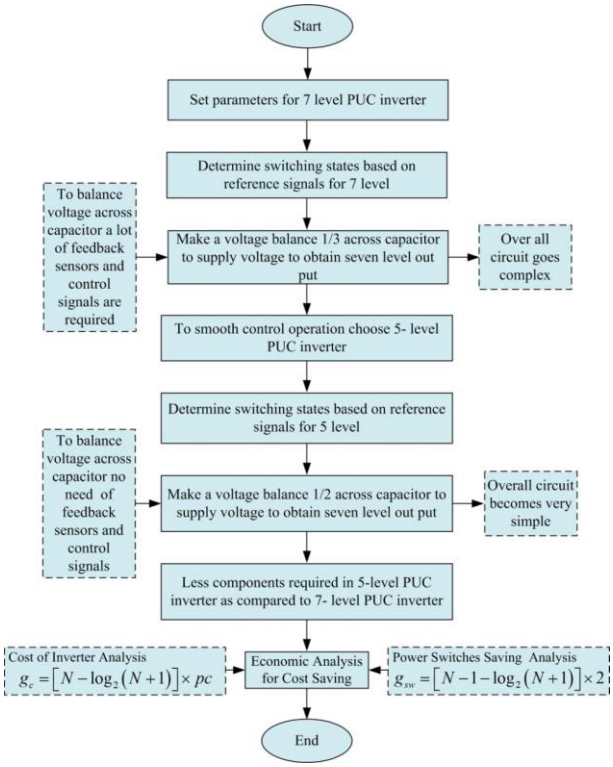

Figure 1. Flowchart of the proposed approach.

The above steps are contained in the flow chart algorithm, as described in **Figure 1**. Initially, we set all the parameters of the seven-level inverter; after that, in the next step, we need to design a controller to control the switches as per desired with advanced control techniques using sensors and other components to balance the capacitor voltage by 1/3 of the source voltage. So that it can be obtained from seven levels on the outside. Due to the increasing excess number of devices for this type of controller, designing the circuit becomes so complex and is avoided by industries for application purposes. Then we again go to the next step to design the PUC5 level controller for smooth operation. After that step, we try to balance the capacitor voltage ½ of the supply voltage. This can be achieved easily without the use of a complex controller circuit. It means the controller design for five levels becomes very simple. Further, in the next step, we can analyze the cost of the inverter, which is directly dependent on the number of capacitors used. As we go above the 7-level, the capacitor counts also increase. The cost of the PUC series inverters depends directly on voltage levels.

3. Realization of PUC 7-Level Multilevel Inverter

The word "U-cell" is frequently used in reference to multilevel inverters. An inverter with a U-shaped power circuit is commonly referred to as a U-cell inverter (Siddique et al., 2019). There may be benefits to this structure in terms of power quality, dependability, and efficiency (Siwakoti et al., 2019). The topology looks like packed U cells. Two power switches and one capacitor make up a single U cell, as shown in **Figure 2**.

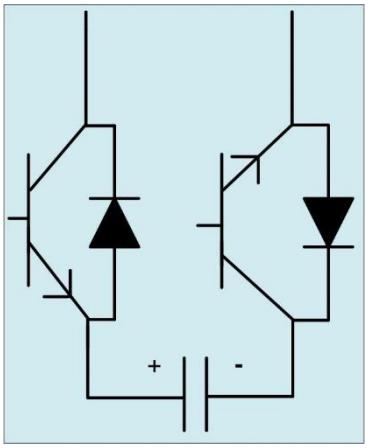

Figure 2. Representation of single U cell.

Power semiconductor devices, like IGBTs, are arranged in U-cell designs according to a certain topology (Yuan, 2016). The main aim of U-cell architecture is to maintain a balance between complexity, losses, and component count. This inverter basically consists of only six switches, a single DC source, and a single capacitor. The voltage across the capacitor is controlled to be fixed at one-third of the first DC source. This topology offers good power quality (Norambuena et al., 2017).

This is the transformer-less single-phase seven-level inverter, as mentioned in **Figure 3**. The (V_{dc}, $2V_{dc/3}$, $V_{dc/3}$, 0, $V_{dc/3}$, $2V_{dc/3}$, V_{dc}) generates the output voltage. To achieve these levels, the capacitor voltage (V_2) must be controlled to $V_1/3$. The number of voltage levels is represented as:

$$Un = a \times u_{(n-1)} + b \text{ and } u_0 = U \quad (1)$$

The n^{th} term is represented as:

$$U_n = a_{U+b}^n \frac{1-a^n}{1-a} \quad (2)$$

$$N_i = 2^{N_{ci}+1} - 1 \quad (3)$$

where,
N_{ci} = number of used capacitors
N_i = number of voltage levels, where '*i*' is an integer.

The switches count N_{swi} obtained by the equation as given below:

$$Ni = 2^{(Nswi/2)} - 1 \quad (4)$$

As the capacitor count increases, the voltage level increases. **Figure 3** shows the holding voltage of T1, T2, and T3 switches with V_1 = 150 V and V_2 = 50 V. The overall AC voltage V_{ab} is, $V_{ab} = V_{aa1} - V_{a2a1} - V_{ba2}$.

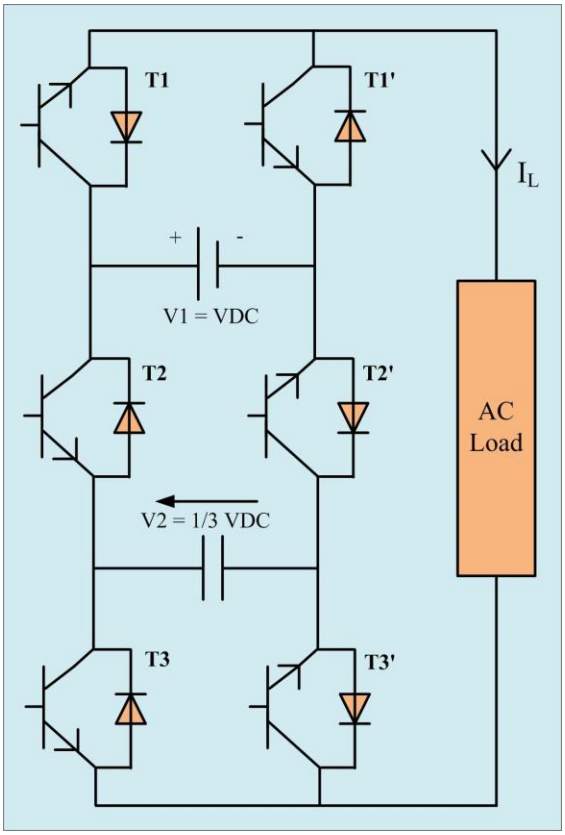

Figure 3. Seven-level PUC inverter circuit.

3.1 Working Operation of PUC 7-Level Inverter

This converter basically consists of two capacitors. One V_1 is a DC source that is created by an AC supply, and the second V_2 is a DC source that is controlled by a control circuit to maintain the desired voltage level (Gupta et al., 2015). The topology consists of six switches: T1, T2, T3 and T1', T2', T3'. Each switch has two operating states that consist of an IGBT with an anti-parallel diode. The three switches on one leg make it possible to define eight possible state combinations.

In these states, two conditions are unessential that is zero voltage, and the remaining six states are to find suitable output voltage levels, as noticed in **Table 2**. **Figure 4** depicts the sequence of all eight possible states (Chitra and Himavathi, 2015). As mentioned, the load is fed by seven-levels V_1, $V_1 - V_2$, V_2, 0, $-V_2$, $V_2 - V_1$, and $-V_1$, for a single-phase topology. The sinusoidal waveform is subdivided into three positive and three negative zones, as shown in **Figure 6**, which are generated by the modulation scheme as shown in **Figure 5**. Seven-stage voltages can be obtained using the switching table (**Table 2**). The circuit Simulink model of this inverter is indicated in **Figure 7**, and its corresponding voltage waveform is shown in **Figure 8**. The comparison has been analyzed with this same level of normal inverter in **Table 3**.

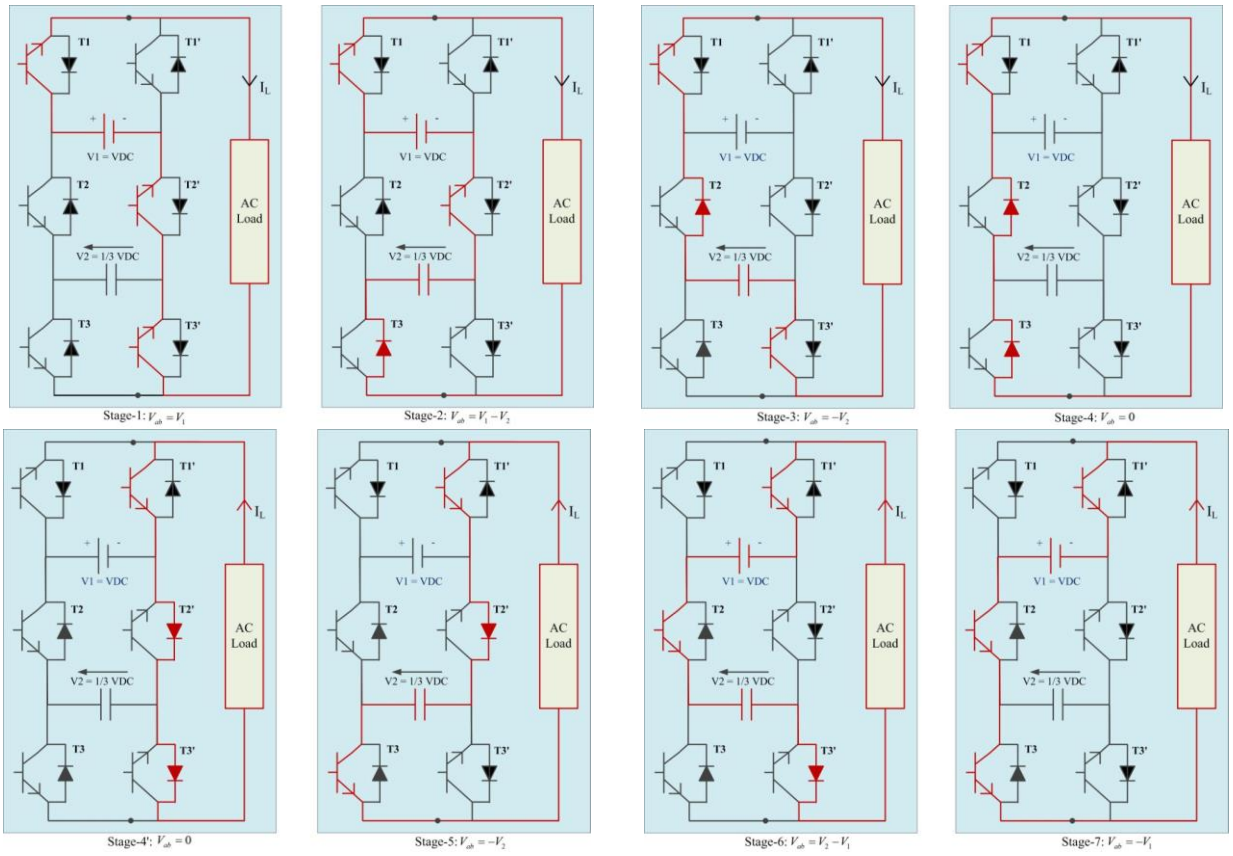

Figure 4. Packed U-cells seven-level topology operating states.

Table 2. PUC seven-level inverter switching table.

State	Signal	V_{ab}	T1	T2	T3
1	5	V1	1	0	0
2	4	V1-V2	1	0	1
3	3	V2	1	1	0
4	2	0	1	1	1
4’	-2	0	0	0	0
5	-3	-V2	0	0	1
6	-4	V2- V1	0	1	0
7	-5	-V1	0	1	1

3.2 Performance Analysis of PUC 7-Level Inverter

A seven-level PUC inverter that is designed with the help of MATLAB /Simulink and the output voltage and current waveforms are shown in **Figure 7**. The proposed modulation scheme is designed as shown in **Figure 5**, with the help of six carriers and one reference sine wave in a phase disposition manner (Tan et al., 2016). In this control technique, there are basically two important things one is carrier signals and the second is reference signals to obtain PWM phase disposition. The reference wave may consider any periodic signal like a sine wave and carrier signals are high-frequency signals like triangular wave or saw tooth wave. In this PUC7 control method, triangular waves have been taken as carrier signals. The reference signal operated at a particular frequency. The reference wave determines the duty ratio and width of the pulse that is generated by comparing both reference wave and sine wave signals. That is directly touch the required power or voltage delivered to the load side. The carrier signals that we considered are high-frequency signals. Also, the carrier signals are much higher frequency signals as compared to the reference signal. The advantage of the PUC7 inverter is that it contains the bi-directional power flow to make it useful for applications in renewable energy areas.

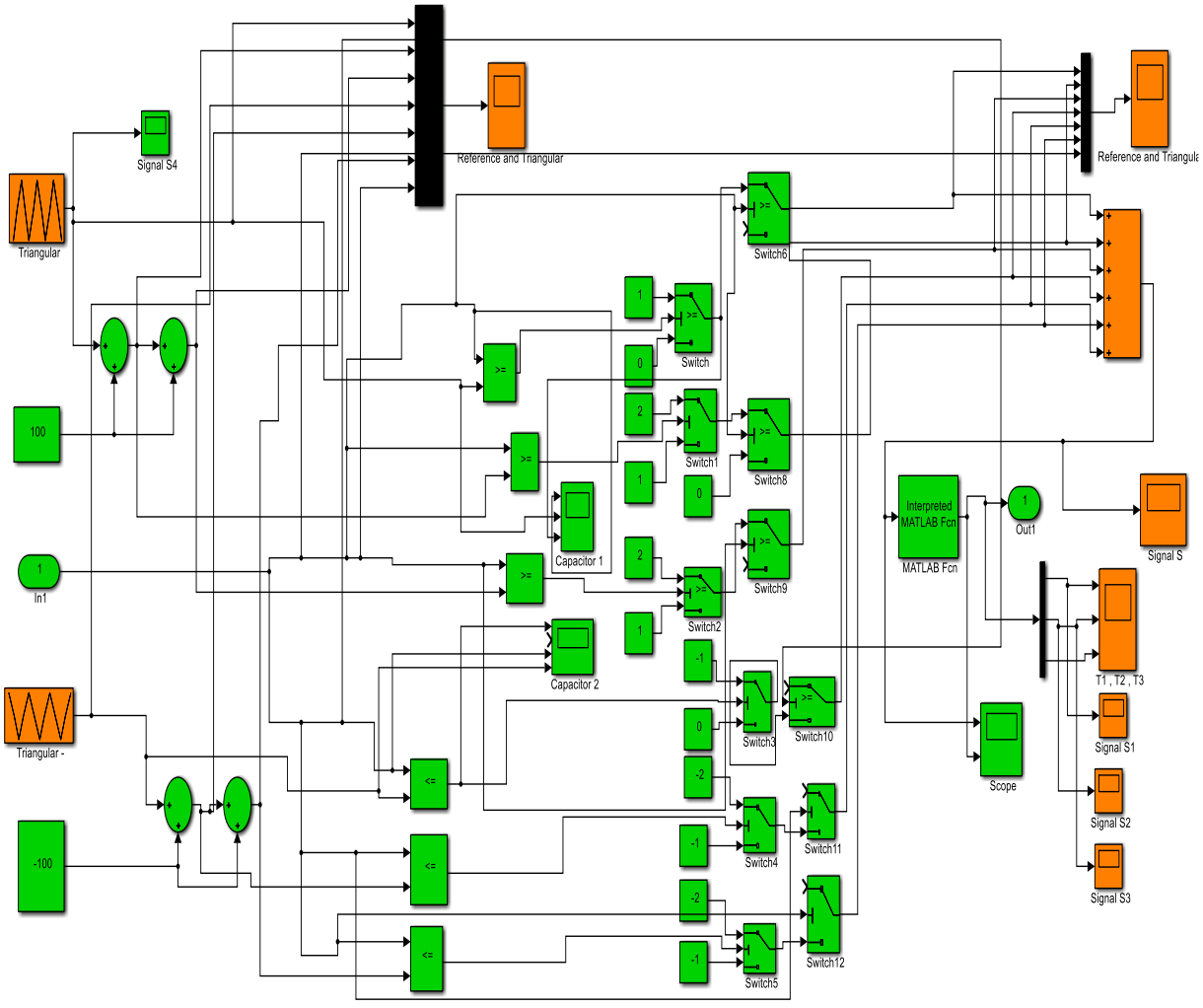

Figure 5. Proposed SPWM modulation.

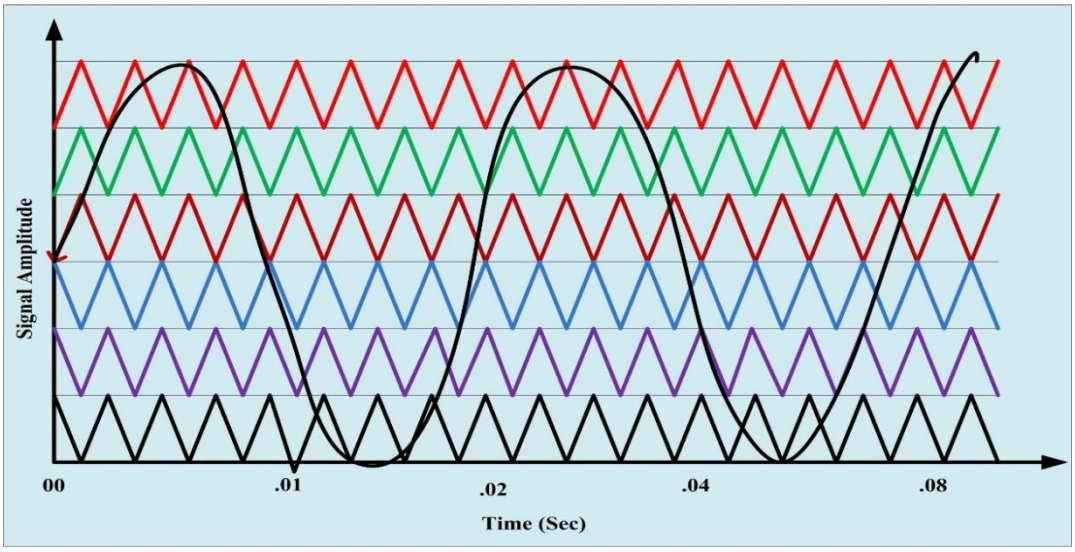

Figure 6. Carrier signals for 7 level inverters.

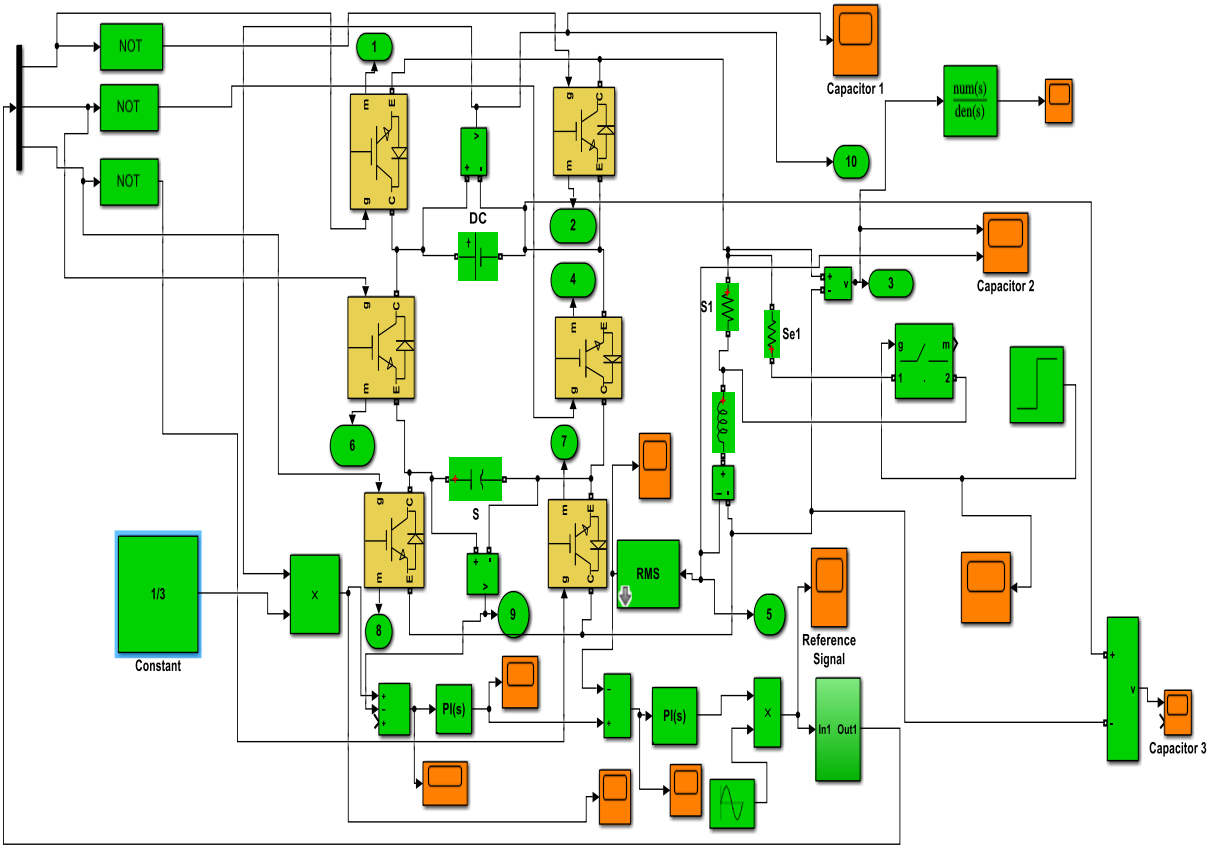

Figure 7. Packed U cell 7 level inverter.

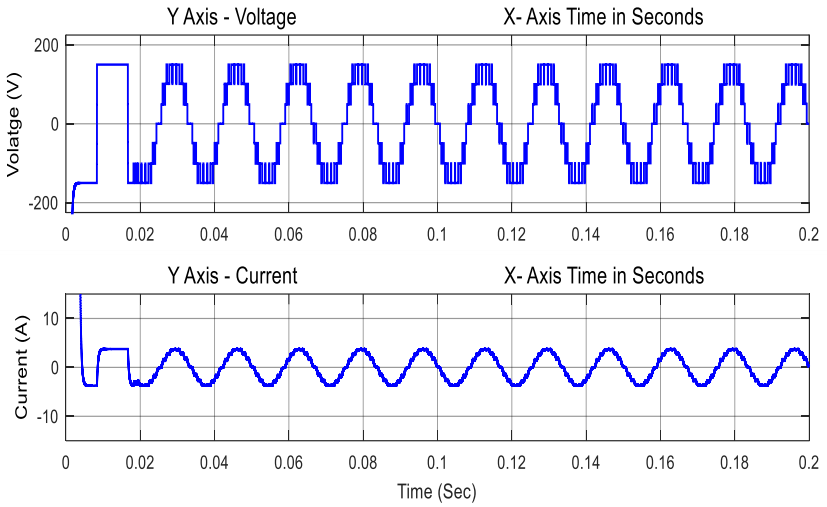

Figure 8. Output voltage and current waveform of PUC7.

Table 3. Comparison of PUC seven-level topologies to other topologies.

Components	Diode clamped	Flying capacitors	Classic cascaded H- bridge	PUC topology
Capacitors	6	6	3	1
Diodes	10	0	0	0
Switches	12	12	12	6

4. Realization of PUC 5-Level Inverter

The PUC 5 inverter is a new mode of operation. First, the PUC inverter proposed for seven levels, in this section it is presented and describes a five-level inverter that can perform in stand-alone and grid-connected modes with suitable and reliable dynamic performance (Saeedian et al., 2018).

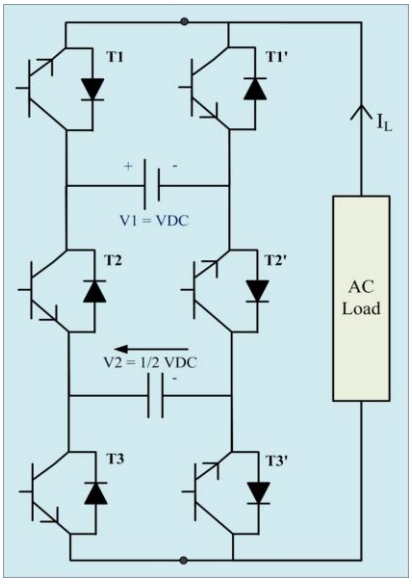

Figure 9. PUC 5 inverter circuit.

This topology is designed for a 5-level PUC inverter as indicated in **Figure 9**. It is based on sensor-less voltage regulation on redundant switching states. The capacitor voltage is charged at half the DC source voltage with the controller to generate the five-level voltages with lower harmonic. This inverter contains six switches one DC source and one capacitor (Siddique et al., 2020a). Basically, the PUC5 inverter is a single-phase topology including complete switching states. This type of inverter is basically governed by a new switching scheme using the help of a sensor-less-based controller.

4.1 Voltage Control Switching Technique

For harmonic reduction, this is a very successful technique. In this approach, only the pulse width may be changed; the pulse magnitude will remain fixed. The carrier wave is compared to the sine wave as a reference signal, resulting in gate pulses. This control method gives the complete desired output voltage with a reference wave connected to the triangular carrier waves (Letha et al., 2016).

The switching strategy of five levels using four carriers (C_{r1}, C_{r2}, C_{r3}, and C_{r4}) wave and sinusoidal reference (V_{ref}) waveform as in **Figure 10**. According to switching states 1, 2, 3, 4, 5, 6, and 8 as shown in **Table 4**, the firing pulses associated, are generated by comparing V_{ref} and carrier waves. To minimize switching frequency, redundant states 4 and 5 are used. If V_{ref} is positive, the output is zero for state 4 and if it is negative, the output is defined as zero for state 5 (Chen et al., 2019).

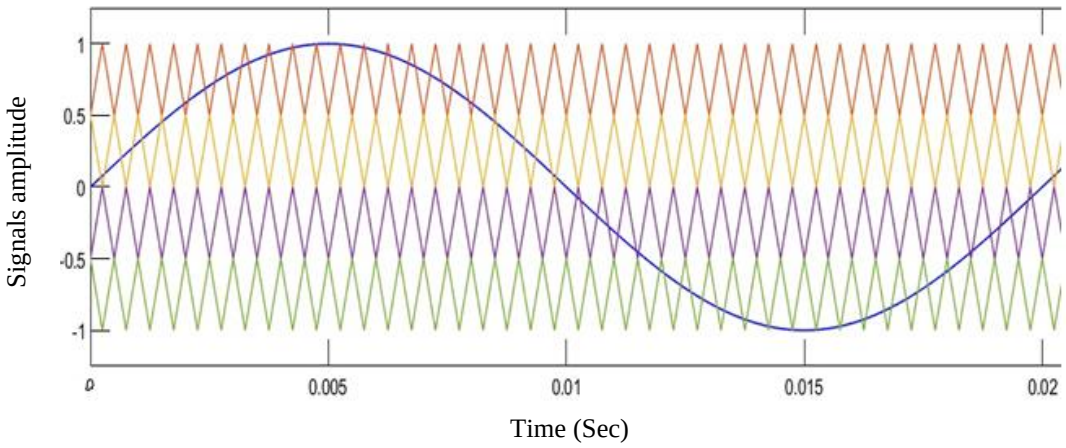

Figure 10. PUC 5-level switching scheme.

4.1.1 Development of 5-Level SLPUC Self-Voltage Balancing Switching Controller

Figure 11 illustrates the algorithm that is described. It can fix the voltage across the capacitor at the required level without the need for a feedback sensor, so the outcome of this inverter offers good output voltage at a low switching frequency (Babaei et al., 2015). The suggested algorithm, when applied to a PUC5 inverter it produces a 5-level voltage waveform output without the need for voltage sensors or integrated controller calculations. Even during startup and during circumstances where the load varies, the capacitor voltage would remain constant. No doubt controller design for seven-level is interesting due to generating a seven-level output voltage by using less component counts. However, the controller becomes complex due to the use of so many feedback sensors for producing a symmetric voltage output waveform. One of the biggest issues for PUC7 is the voltage balancing problem when we go for a high switching frequency for this converter.

So, to investigate this type of problem, the 5-level PUC new switching technique is designed for implementation in high switching frequency and medium power applications. For the design of the PUC5 controller, there is no need to add additional control components to make a complex controller design. The best you can expect from this controller is that if it is integrated with switching frequencies, it will give very high and dynamic performance. The overall advantage of this controller is its simplicity in design and the lack of a need for voltage-balancing components. In the PUC5 inverter, the redundant switching states are properly designed as per the requirements of the PWM method. All the switching states are designed on the basis of capacitor effects.

In a self-voltage-balancing mechanism using multicarrier PWM as from **Figure 11**, the SLPUC inverter capacitor voltage is set at half of the DC source amplitude. The lack of complex controllers, and no need for voltage or current sensors. With less harmonic distortion, the output voltage waveform of PUC5 is symmetrical and the capacitor voltage is kept steady at the desired level (Siddique et al., 2019).

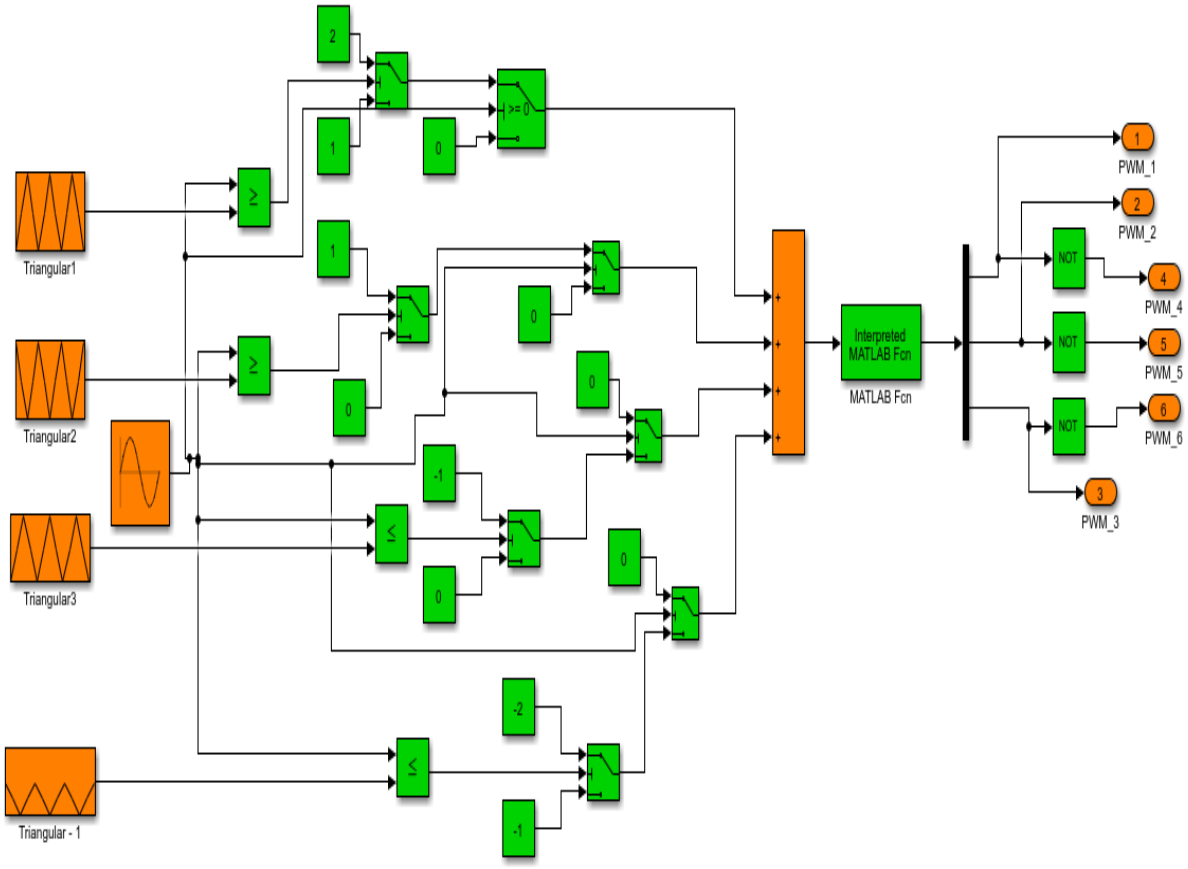

Figure 11. Proposed open-loop switching scheme of PUC5 Inverter.

4.1.2 Operation of PUC 5-Level Inverter

Figure 12 indicates the single-phase PUC inverter. **Table 4** lists all possible switching states. Each of these eight states provides a different path for the flow of current. The PUC inverter operates as a five-level inverter (**Figure 12**) by adding $V_1=2V_2=2E$, so the waveform of the 5-level inverter includes the levels 0, ±E, and ±2E. The capacitor voltage (V_2) makes up half of the DC source (V_1). To manage the capacitor

voltage, half of the DC sources the capacitor charge and discharge through redundant switching states. So, for using the excess states, the well-constructed (required for) PWM scheme for this inverter (Siddique et al., 2020b). All paths created by switching states are described below in **Table 5** and are shown in **Figure 13**.

Based on **Figure 13**, for switching states, the DC source and capacitor are connected in series with the load, and the capacitor charges (states 2 & 7). It is discharging (states 3 & 6). In the rest of the states, the capacitor voltage remains unchanged and is not connected to the DC source and load. **Table 6** indicates the states of operation of the capacitor in both charging and discharging modes.

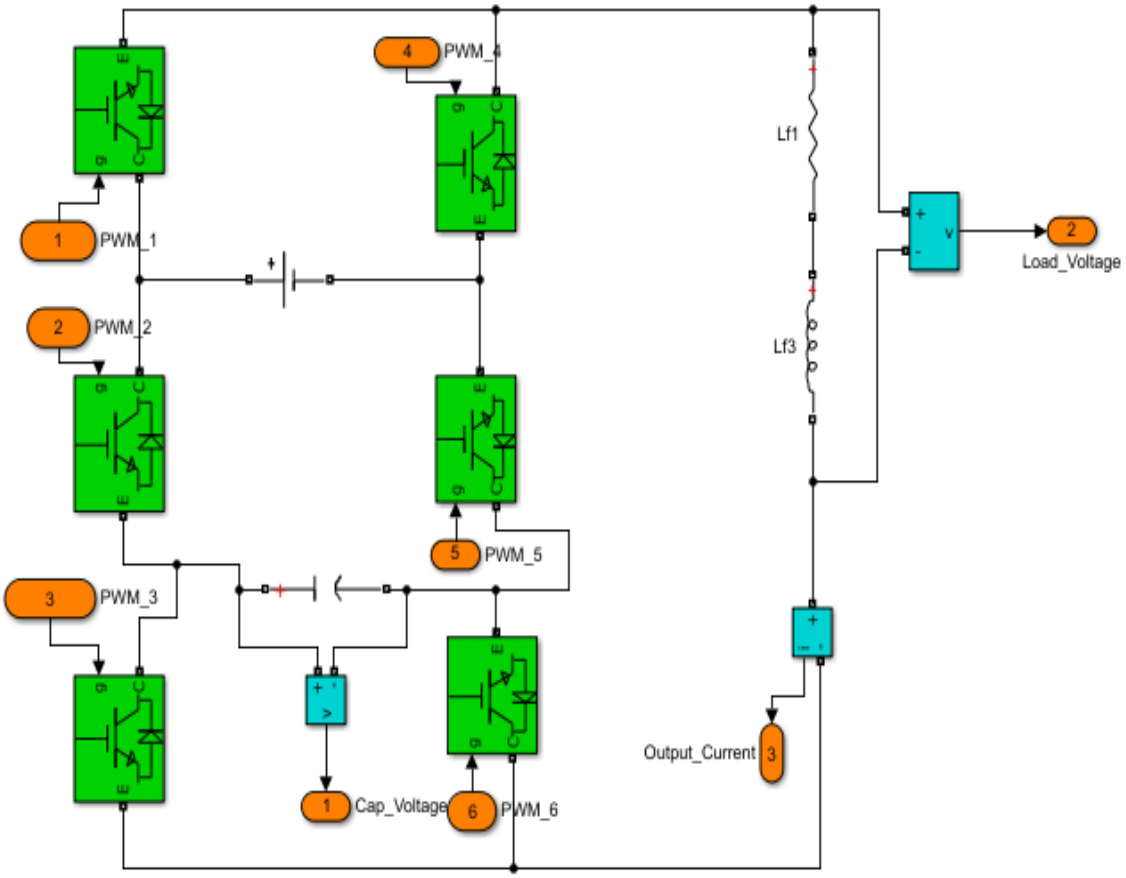

Figure 12. PUC 5 inverter model.

Table 4. All possible switching states of PUC 5 inverter.

State	S1	S2	S3	Output Voltage
1	1	0	0	V_1
2	1	0	1	V_1-V_2
3	1	1	0	V_2
4	1	1	1	0
5	0	0	0	0
6	0	0	1	-V_2
7	0	1	0	$V_2 - V_1$
8	0	1	1	-V_1

Table 5. All voltage levels generated by 5-level PUC inverter.

State	S_1	S_2	S_3	Output voltage	V_L
1	1	0	0	V_1	+2E
2	1	0	1	V_1-V_2	+E
3	1	1	0	V_2	+E
4	1	1	1	0	0
5	0	0	0	0	0
6	0	0	1	-V_2	-E
7	0	1	0	$V_2 - V_1$	-E
8	0	1	1	-V_1	-2E

Table 6. Voltage states of capacitor.

State	Capacitor voltage
1	No Effect
2	Charging
3	Discharging
4	No Effect
5	No Effect
6	Discharging
7	Charging
8	No Effect

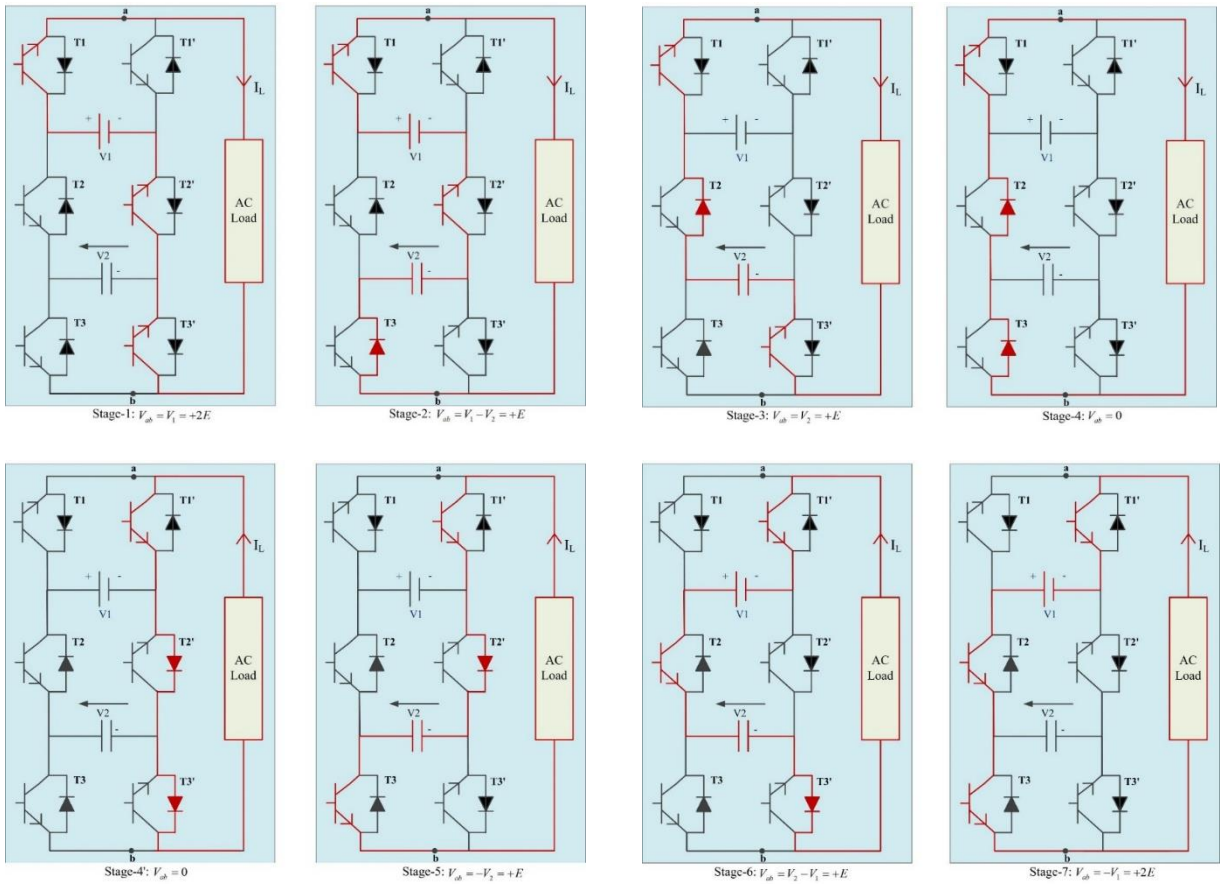

Figure 13. Conducting paths of 5-level PUC inverter.

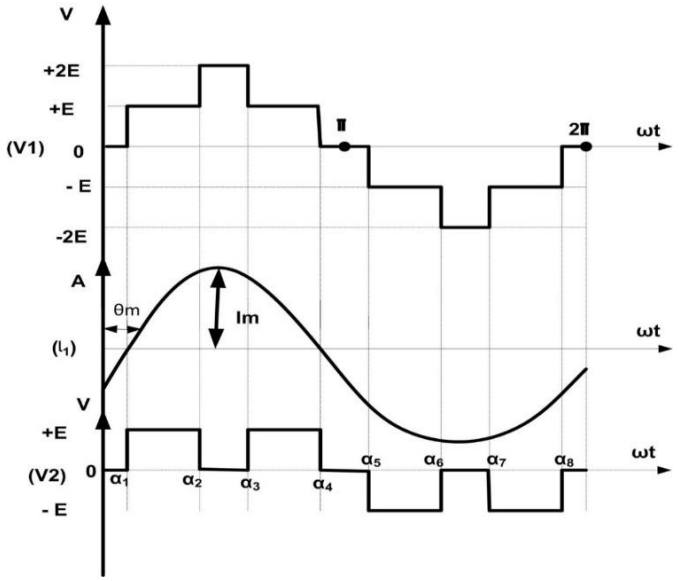

Figure 14. One cycle five-level inverter's output voltage and current waveform.

4.2 Performance Analysis of PUC 5-Level Inverter

The PUC5 inverter is tested in a variety of load scenarios, including stand-alone mode and UPS applications with load and DC source changes. This type of inverter is applied to the RL load in this mode (Bose, 2008).

When the DC source voltage changes and the capacitor voltage correctly tracks the reference value ($V_1/2$), the voltage balancing waveform across the capacitor, five-level inverter output voltages, and load current are indicated in **Figure 15**, as a result of the suggested sensor-less voltage regulator technique incorporated into the switching pattern. The results have been tested using MATLAB/Simulink setup.

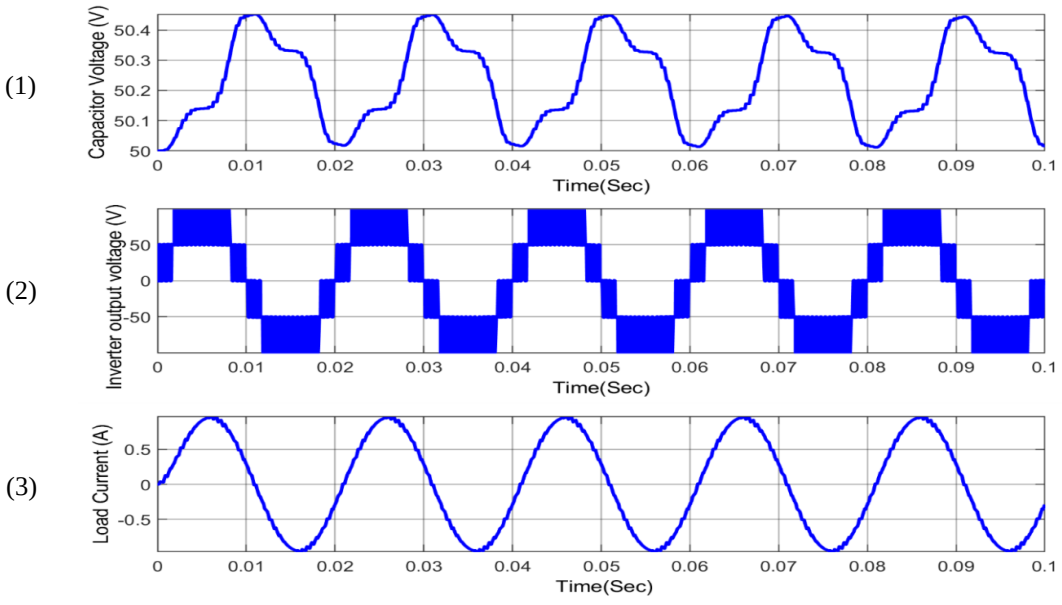

Figure 15. Waveform representation of 91) Capacitor voltage, (2) Load voltage, (3) Output current.

This technique is not based on feedback sensors for the device model. It can run the device from zero voltage to arbitrary amplitude and in situations of the variance of the DC source voltage as well.

5. Economic Analysis for Cost Saving

Basically, the cost directly influences the number of components used in inverters. The PUC base inverters take fewer components as compared to other same-level hybrid inverters. As we know, in PUC base inverters, the number of levels depend on the number of capacitors used. The Flying Capacitor (FC) topology needs 12 switches and six capacitors for seven levels; whereas PUC 7 generates seven levels with a 200% of cost reduction in terms of passive components and 100% in terms of active components. By this method, the number of switches has been minimized from twelve to six, and the capacitor's count has been reduced from six to one. Consequently, the FC 5 level topology needs 8 switches and 3 capacitors for five levels, when compared with the U-cell 5 level topology, the cost reduction is 150% in terms of passive components. The PUC 5 and PUC 7 level inverters are smaller in size, resulting in very compact power conversion units (Sandeep and Yaragatti, 2017).

The cost savings are incorporated in terms of capacitors and voltage levels. **Figure 16** indicates the voltage level in terms of the percentage cost of the inverter. In the same manner, as shown in **Figure 17**, the number of capacitor requirements in an inverter depends on voltage levels. As the level goes up, the capacitor requirement also goes up. So, the cost of high-level inverters increases in terms of the increases in active and passive elements (Khenar et al., 2018).

The cost of the inverter depends on inverter levels in terms of capacitor that is obtained from the equation:

$$g_c = (N - \log_2(N + 1)) \times pc \tag{6}$$

where,
pc = price of single capacitor
N = inverter level.

This cost percentage can be expressed by,

$$g_c(\%) = \frac{100 \times N - \log_2(N+1)}{\log_2(N+1) - 1} \tag{7}$$

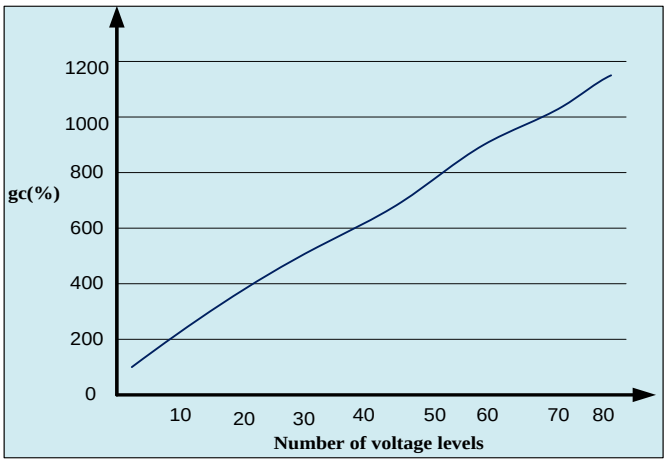

Figure 16. Cost saving in (%) in terms of capacitors as per voltage levels.

The equation for saving switches

$$g_{sw} = \left(2\times(N-1-\log 2(N+1)\right) \quad (8)$$

$$N = Nc + 1 \quad (9)$$

The power quality gain equation:

$$g_q = 2^{Nc+1} - N_c - 2 \quad (10)$$

where, Nc = number of capacitors.

Using this topology instead of flying capacitor increases the voltage levels by a factor of two for the same number of capacitors.

$$g_1(\%) = \frac{2^{Nc+1} - Nc - 2}{\log_2(N+1) - 1} \quad (11)$$

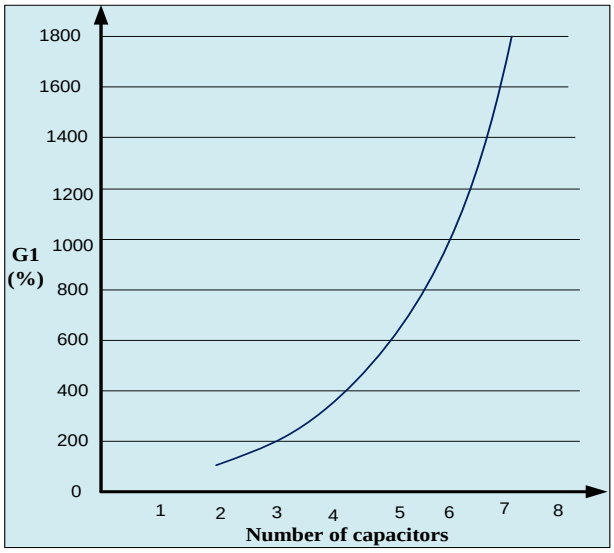

Figure 17. Power quality gain in (%) in terms capacitors count.

6. Comparison Analysis of PUC7 and PUC5 Inverters

The sensor less PUC 5 inverter is compared in the context of component requirements to other same-level inverters and the complexity of the control strategy. Basically, the PUC5 inverter uses one redundancy in the switches. As we know, it balances the voltage level by half across the capacitor. So, there is no need to sense the voltage across the capacitor, and due to this, there is no control of voltage ripple, so it allows to go with a big capacitor DC link. There are so many technologies used to control the capacitor voltage. In this technology, it is not easy to go to higher levels due to voltage balancing issues, so it is a considerable task. In this paper, also PUC 7 is introduced because, by considering a single source, we can go to a to a higher level, and its output only depends on the auxiliary capacitor that is always used in this technology for voltage balancing purposes. To control PUC7, there may be a high switching frequency required for controlling the voltage across the capacitor by using current sensing controllers. This technology is very high-speed and has variable switching frequencies. It is not used as a grid-connected mode, while PUC5

can be used as a grid-connected mode. The industries also do not recommend this technology for commercial purposes. So, by getting some modifications in technology, the 5-level voltage can be generated, and it is a very simple and easy procedure by considering redundancy in the switches. One more advantage of the PUC5 inverter is not only balances the voltage but also maintains THD as per the PUC7 level with a simple modulation technique.

One of the challenging issues of these inverters is the equal voltage sharing of switches, and the PUC5 inverter is designed for equal rating switches to equal voltage sharing. The two switches of the above side share 2E voltage, while the remaining four switches share an equal amount of voltage. There are similarities between the PUC5 and CHB inverters. The PUC5 voltages are connected in series to achieve a high output voltage as well as a higher level. By connecting two PUC5 inverters, it can achieve 25 levels. After reviewing, it shows that PUC 5 is a much preferable inverter as compared to PUC7 due to its very less complex control structure. While PUC7 contains much complex algorithm for voltage balancing, and performance-related, also PUC 5 can used in both standalone and grid-connected modes as compared to PUC7, which is not preferred for the same mode. Basically, the PUC series incorporates more voltage levels, and the seven-level topology is a transformer less topology. While other types of inverters, like cascaded H-bridge, and diode-clamped inverters, need a large number of transformers. A PUC-based inverter is used to minimize the switches and sources. Comparisons are as follows:

- The PUC5 inverter is sensor less inverter, while the PUC7 is sensor-based inverter.
- In compare to all same level inverters PUC7 & PUC5 inverters contains fewer components.
- A lot of feedback sensors and other control components are needed to balance voltage in the PUC7 inverter while in the PUC5 inverter no voltage balancing issues so no need for external control components.
- The control complexity of PUC7 is high than PUC5 inverter.
- The PUC5 inverter is very economical and easy to operate as compared to the PUC7 inverter.

Table 7. Single phase 5-level inverter components.

Inverter Type	DC Source	Capacitor	Diode	Switch	Total Parts	Feedback sensors	External control components	Control Complexity	Cost
PUC7	1	1	0	6	8	Require	Required	High	High
PUC5	1	1	0	6	8	No Required	No required	Very Low	Low

It is found that, in comparison to the PUC7 inverter, the PUC5 inverter requires very few components and very low control complexity, as mentioned in **Table 7**.

7. Conclusion

Higher-level inverters are typically more expensive and sophisticated. More powerful electronic parts, control circuits, and frequently more advanced modulation techniques are needed for the higher levels. Maintenance and dependability may be impacted by the complexity. One important consideration is an inverter's efficiency. Even though a 7-level inverter might provide higher-quality output, it's important to take the overall efficiency into account, taking into account losses in the control systems and additional components.

In contrast to the proposed 5-level PUC inverter, the PUC 7 inverter requires a complex controller to achieve as per required voltage levels, so it requires modifying a greater number of controller gains in operation.

The development of the desired controller requires a significant amount of time and effort in accurately modeling the device and employing multiple state variable feedbacks, which increases the number of state variables and, as a result, the number of voltage and current sensors, which are necessities to maintain as the desired output voltage. It may produce incorrect results with a larger number of spikes on the induced voltage waveform, so the additional protection requirement increases as compared to the PUC 5 inverter. Overall, the PUC 7 inverter does require further research and development to make it useful in every condition. The performance of the PUC5 inverter, on the other hand, results in a less complicated controller, less switching frequency, very low power losses, faster dynamic performance, easier operation, and more stable behavior. Overall, it is clear that the PUC5 inverter is designed to depend on the charging and discharging of the switching frequency, not on the system frequency. So, an appropriate algorithm is designed to cover all states to balance the voltage of PUC5, and there is no requirement for sensors for this. All of these benefits arise from the proposed 5-level SLPUC inverter-designed switching pattern, as well as the fact that this topology requires fewer components.

Depending on particular application requirements, such as the intended output waveform quality, system efficiency targets, and the allowable degree of control complexity, one may choose between a PUC 5 and a PUC 7 inverter. Applications requiring greater voltage precision and less harmonic content would be chosen for a PUC 7 inverter, while those requiring a better balance between complexity and performance might favor a PUC 5 inverter. Packed U Cell 5-level inverter: "In addition, there might have been modifications to industry norms or technological breakthroughs.

Conflict of Interest

There is no conflict of interest

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